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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/523,990	03/13/2000	Mou-Shiung Lin	MEG99-005	6138

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EXAMINER	
WALSH, DANIEL I	

ART UNIT	PAPER NUMBER
2887	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/523,990	LIN ET AL.	
	Examiner	Art Unit	
	DANIEL I. WALSH	2887	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44,48,49 and 60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44,48,49 and 60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt is acknowledged of the Amendment received on 2-7-08.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 44, 48, 49, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al. (US 6,476,499) in view of Hiromasa (JP362169448A), as cited in a previous Office Action.

Hikita et al. teaches a circuit component comprising a substrate, a semiconductor chip having a front surface and a back surface wherein said front surface comprises multiple pads, wherein said front surface is on a bottom of said chip and wherein the back surface of the chip is

on top of the chip; a machine readable information directly on said back surface of the chip wherein said machine readable is an identity of product and manufacturer or said machine readable information is a bar code; multiple metal bumps directly on said multiple pads of said chip wherein said bumps attach the chip to a top surface of said substrate as bumps are used to bond the chips (1,2) to each other via electrodes (13,23). It would have been obvious to use metal bumps/solder for conductivity, as is conventional in the art.

Hikita et al. is silent to an optically transparent layer directly over said back surface that covers the identity of product and manufacturer or said barcode, wherein the identity of the product and manufacturer or said barcode is machine readable and visible through said optically transparent layer.

Hiromasa teaches a transparent resin on an IC chip package through which identification information can be read (FIG. 1). Though silent to machine readable, it would have been obvious to one of ordinary skill in the art that such notations are capable of being read by machines, in order to provide increased accuracy/efficiency by replacing manual reading with machine reading, which involves only routine skill in the art. The mere claiming that information appears machine readable does not appear to effect the structure of the device, as the Examiner believes that identification information such as chip markings are capable of being machine read, as is indicia, and the specifying of a particular type of information appears an issue of printed matter, as the indicia is not functionally related to the device, and as such, the printed matter is not patentable as it merely provides information and therefore is a matter of design choice/variation

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hikita et al. with those of Hiromasa in order to apply the teachings of transparent protective coatings over identification information

One would have been motivated to do this in order to protect/cover the information while still permitting it to be read. As transparent it is believed to permit machine reading.

Though Hikita et al. teaches removing of mold in order to read/inspect packages, the Examiner notes that as Hiromasa teaches a transparent resin top/mold, the information can be viewed without requiring mold removal, thus providing such prior art elements according to known methods would yield predictable results, such as reduction of steps/increased efficiency while also providing more chip package protection.

Re claim 48, Hikita et al. teaches a mold package (col 17, lines 55+). Though silent to an underfill between the front surface and a top surface of said substrate that encloses the metal bumps, the Examiner notes that is it well known and conventional in the art that such mold packages can be interpreted as an underfill material encloses bumps and parts of the circuit/package. One would have been motivated to do so in order to protect/cover elements.

Re claim 49, though silent to balls on a bottom surface of said substrate, the Examiner notes that balls on a surface are an obvious expedient, well within the ordinary skill in the art, to effect connection between elements. The Examiner notes that balls/bumps are conventional to attach substrate together, as in flip chip/stacked chip arrangements.

4. Claims 48, 49, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hikita et al./Hiromasa, as discussed above, in view of Flip Chip, as discussed in the previous Office Action.

The teachings of Hikita et al./Hiromasa have been discussed above.

Hikita et al. /Hiromasa are silent to the underfill, balls on the bottom of the substrate, and solder bumps.

Flip Chip teaches such limitations (see lone drawing).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hikita et al. /Hiromasa with those of Flip Chip.

One would have been motivated to do this in order to use known techniques to produce predictable results, such as underfill/protection/covering of elements and connectivity (conductivity)between elements, as bumps/balls of metal/solder are known in the art to effect connectivity between elements, and underfills are known to provide protection/covering.

5. Claims 44, 48, 49, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hyozo et al. (US 5,894,172) in view of Hiromasa, as discussed above, and Flip Chip, as discussed above.

Hyozo et al. teaches a chip with a front and back surface where the front surface is a bottom and the back surface is a top, and machine readable information directly on said back surface of the chip (FIG. 8). The Examiner notes that the type of information selected is a matter of design variation, not functionally related to the substrate and therefore is not patentable. The information 8 is interpreted as machine readable, motivated for increased efficiency and accuracy (machine reading).

Hyozo et al. is silent to the chip being a flip-chip/the structure of pads, bumps, solder, substrate, and underfill as claimed.

Flip Chip teaches such limitations, as discussed above.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hyozo et al. with those of Flip Chip.

One would have been motivated to do this to provide identification information on the chip (directly on the chip) that can be printed on the surface of the chip in various location, since no electronics circuit devices are connected on that surface of the chip. Applying such identification information to a flip-chip structure would enable known techniques to be provided on similar devices in a same way to produce predictable results, namely direct application of identification information.

Hyozo et al./Flip Chip are silent to a transparent encapsulant.

Hiromasa teaches such limitations (as discussed above).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Hyozo et al./Flip Chip with those of Hiromasa in order to apply the teachings of transparent protective coatings over identification information.

One would have been motivated to do this to protect the information while still permitting it to be read (transparent).

The Examiner notes that the claming of information being machine readable, does not appear to effect the structure, as it is understood that the information can be read through the transparent coating,

Response to Arguments

6. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

7. The Examiner notes that information is interpreted as capable of being machine readable, since it is well known and conventional in the art that manually read information can be machine read, such as to improve speed/accuracy. Additionally, merely claming that information is machine readable, does not appear to affect the structure.

8. In response to the Applicants arguments regarding direct application of the information on the chip, as set forth in the office action above, identification information is applied directly onto chip elements. Further, the Examiner notes that transparent encapsulates and other coatings are well known and conventional in the art, to protect/coat. The combination of indicia directly on a chip, with transparent coatings would result in expected results such as protection while still permitting readings.

9. In response to the applicants arguments regarding the type of information/indicia, the Examiner notes that the type of information is an issue of printed matter, and as such, is not function related to the substrate, and therefore merely provides a type of information. This appears a matter of design choice, and therefore such printed matter is not patentable. As prior art with printed information has been taught above, the type of information specifies is therefore an obvious matter of design variation.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure (See PTO-892 for various examples of protective coatings and indicia applied onto chips/packages).

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL I. WALSH whose telephone number is (571)272-2409. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Paik can be reached on (571) 272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Daniel I Walsh/
Primary Examiner
Art Unit 2887